In the Specification:

Please amend the paragraph at page 6, line 18 – page 7, line 6, as indicated below.

In a related embodiment, implementing the ultra low power UART mode involves significantly reducing or deactivating (TL1 = 0) the first clock signal. TL1 is reduced to zero by multiplexer 64 in selecting a signal in response to the clock control signal received from CPU 40. In this example, CPU 40 converts to a sleep mode for a predetermined time period, but serial data 12 would continue at the second clock rate (TL2). In another example embodiment, arrangement 10 operates in an enhanced-performance mode by increasing TL1 with respect to TL2. In this example, multiplexer 64 receives a control-signal instruction from CPU 40 to select a higher clock rate from divide-by-N circuit 62 such that TL1 is greater than TL2. In this example, CPU 40 and a portion of UART chip 20 now operate at the new timing level to process data faster than at the previous level, while the rate of serial data streaming into UART chip 20 remain unchanged.

Please amend the paragraph at page 7, line 18 – page 8, line 3, as indicated below.

Referring now to FIG. 2, circuit arrangement 100 illustrates an expanded implementation of UART chip 20 as per FIG. 1. UART chip 20 encompasses a parallel bus interface circuit 101 having a bus buffer 102, an operation control circuit 104 and an interrupt control circuit 106. Bus buffer 102 is responsive to operation control circuit 104 and allows read and write operations to occur between CPU 40 and UART chip 20. Operation control circuit 104 receives operation commands from the CPU and generates signals to internal sections of the UART to control UART operation. Interrupt control circuit [[104]]106 provides an interrupt upon an occurrence of a specific event, such as one of the previously-discussed, flow-control conditions.